Prof. Chandra Sekhar Paidimarry received Post Doctoral Fellowship (2009, Shizuoka University, Japan), PhD (2009, OU), M.Tech (1999, JNTUH) and BE (1991, Nagpur University). Presently he is serving as Vice-Principal, University College of Engineering (UCE), OU from 2021. He served as Director of Evaluation, Examination Cell, UCE (2019-21), Head, Dept of ECE, UCE (2012-14 & 2017-19), Chairperson in ECE, BoS (2015-17). He worked in Vaagdevi College of Engineering, Warangal (1999 to 2001). He has been working in Dept of ECE, UCE, OU from 2001 and is elevated as Professor in the year 2015. Prior to joining in teaching, he has eight years of industrial experience of Design and Development of Embedded Systems (1991-99). He is actively involved in establishing the state of art Laboratories in the Department of ECE, OU. Sixteen Doctoral students have completed PhD under his guidance. He has published a patent titled, "**Improved Real-time GPS RF Data Capturing for GNSS SDR Applications**" and more than 50 research publications in peer reviewed journals. He has successfully executed a UGC sanctioned Major Research Project on "**GNSS Receiver: Baseband algorithms in FPGA**", worth of Rs. 15 Lakh. He successfully executed two consultancy projects from DLRL and RCI. MeitY, Government of India sanctioned a prestigious Chip to Start-up (C2S) program worth of 3 Crores to tape out **Novel ADPLL IP Core for BLE Applications** at 180 and 90 nm nodes and train Manpower in the domain of VLSI design. EDA tools, namely Cadence Full Suite, Synopsys, Siemen and Ansys have been procured under the project. MathWorks Pvt Ltd sanctioned a Research Project, Development of Waveform Generators and GNSS Receiver Algorithms, worth 32 Lakhs. Prof. ChandraSekhar has received prestigious **Prof. K. Srinivasan Memorial Award** (2023) from IETE for his outstanding skills in teaching and research. He is also a recipient of best teacher award from Institution of Engineers-India (IEI) (2017), Vice Chancellor award (2022) for excellence in teaching. He was Chair of CAS& EDA Joint chapter of IEEE Hyderabad section. He is presently serving as Editorial Board Member of IETE Journal of Research and IETE Journal of Education. He is a Senior Member of IEEE, Fellow of IETE and IEI. He is presently Executive Committee Member of Gurugram University, Haryana. He is currently serving as Peer review committee member of DLRL projects and Member, System Engineering, BDL. He is member of Board of Studies in several Engineering colleges. He introduced industry demanding courses, namely, VLSI Design & Verification using System Verilog, Hardware Accelerators for Machine learning, Computational EM, Parallel Processing using CUDA/OpenCL etc. His research interests include Analog & Mixed IC Design and Development of Efficient Algorithms using FPGA and Deep Learning.